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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,409	04/19/2004	Robert Louis Hodges	98-P-104D1 (850063.542D1)	2598
30423	7590	11/16/2005	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			SOWARD, IDA M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/827,409

Applicant(s)

HODGES, ROBERT LOUIS

Examiner

Ida M. Soward

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 October 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 1-13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-18 is/are rejected.
- 7) ☒ Claim(s) 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>04-19-2004</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

This Office Action is in response to the election filed October 27, 2005.

### ***Election/Restrictions***

Applicant's election with traverse of claims 14-19 in the reply filed on October 27, 2005 is acknowledged. The traversal is on the ground(s) that first, the Examiner incorrectly stated that the inventions of groups I and II are related as process of making and product made, and second, even if the claims of Group II were process claims, the Examiner has not correctly shown that the product claims of Group I could be made by a materially different process. This is not found persuasive because the claim construction contains the method of manufacturing a semiconductor structure.

The requirement is still deemed proper and is therefore made FINAL.

### ***Specification***

The abstract of the disclosure is objected to because “**comprises**” should have been **includes** in line 1, page 16. Correction is required. See MPEP § 608.01(b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Moslehi (5,322,809).

In regard to claim 14, Moslehi teaches a semiconductor structure 10, comprising: a semiconductor substrate 12; a well 14 in the substrate 12, the well 14 having an opposite conductivity type with respect to the substrate 12; first and second dielectric spacers 32 positioned on the substrate 12 and defining opposite sides of an opening; a gate dielectric 20 positioned on the substrate 12 and in the opening; a gate electrode 22 formed in the opening and on the gate dielectric 20, the gate electrode 22 being limited by the dielectric spacers 32; first and second halos 30 in the well 14 and under the first and second dielectric spacers 32, a channel being defined in the well 14 by the halos 30; and source and drain regions 34 in the substrate 12 and adjacent to the first and second halos 30 (Figure 3d, columns 3-5, lines 6-67, 1-68 and 1-25, respectively). In regard to the well being implanted in the substrate; first and second halos being implanted in the well and under the first and second dielectric spacers, respectively; and the source and drain regions implanted in the substrate and adjacent to the first and second halos, respectively, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The

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patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

In regard to claim 15, Moslehi teaches dielectric isolation structures 18 formed in the substrate 12 on opposite sides of the wall 14 (Figure 3d, columns 3-5, lines 6-67, 1-68 and 1-25, respectively).

In regard to claim 16, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

In regard to claim 17, Moslehi teaches the dielectric spacers 32 having a height that is more than twice a width of the spacers 32 (Figure 3d, columns 3-5, lines 6-67, 1-68 and 1-25, respectively).

In regard to claim 18, Moslehi teaches silicide contacts 40 & 41 formed on the gate electrode 22, source 34, and drain 34 (Figure 3d, columns 3-5, lines 6-67, 1-68 and 1-25, respectively).

***Allowable Subject Matter***

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to gated semiconductor structures:

Bulucea (6,020,227)

Huang (5,572,078)

Jimenez (5,801,078)

Kaneshiro et al. (5,427,964)

Lee et al. (5,292,681)

Tsai et al. (5,648,287).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS  
November 13, 2005

*John M. Sivak*  
*Art 2822*